compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A method comprising:

forming isolation regions in a semiconductor substrate;

etching a portion of the semiconductor substrate between opposite sidewalls of the isolation regions to form a first recess;

epitaxially growing a first silicon germanium layer in the first recess, wherein the first silicon germanium layer has a first germanium concentration;

epitaxially growing a second silicon germanium layer in the recess and over the first silicon germanium layer, wherein the second silicon germanium layer has a second germanium concentration lower than the first germanium concentration;

forming a gate stack over the second silicon germanium layer;

recessing the second silicon germanium layer to form a second recess adjacent the gate stack; and

epitaxially growing a silicon-containing semiconductor region in the second recess to form a source/drain stressor, wherein arsenic is in-situ doped during the step of epitaxially growing the silicon-containing semiconductor region, wherein the silicon-containing semiconductor region comprises silicon germanium stressor having a third germanium concentration lower than the first germanium concentration and the second germanium concentration.

2. The method of claim **1**, wherein in the epitaxially growing the first silicon germanium layer and the second silicon germanium layer, a precursor selected from the group consisting essentially of AsH_3, trimethyl arsenic (TMAs), tertiarybutylarsine (TBAs), and combination thereof is used.

3. The method of claim **1**, wherein the silicon-containing semiconductor region comprises a silicon stressor that is substantially free from germanium.

4. The method of claim **1** further comprising recessing the isolation regions, so that a portion of the second silicon germanium layer forms a semiconductor fin that is above top surfaces of remaining portions of the isolation regions, wherein the gate stack comprises a first portion directly over the semiconductor fin, and a second portion on a sidewall of the semiconductor fin.

5. The method of claim **1**, wherein the gate stack comprises a gate dielectric, and wherein the gate dielectric is in contact with a top surface of the second silicon germanium layer.

6. A method comprising:

epitaxially growing a first silicon germanium layer over and in contact with a portion of a silicon substrate, wherein the first silicon germanium layer has a first germanium concentration;

epitaxially growing a second silicon germanium layer over and in contact with the first silicon germanium layer, wherein the second silicon germanium layer has a second germanium concentration lower than the first germanium concentration;

forming a gate stack over the second silicon germanium layer, wherein a portion of the second silicon germanium layer forms a channel region of an n-type metal-oxide-semiconductor (NMOS) field-effect transistor (FET);

recessing the second silicon germanium layer to form recesses on opposite sides of the gate stack; and

epitaxially growing semiconductor stressors in the recesses, wherein the semiconductor stressors comprise silicon germanium having a third germanium concentration lower than both the first germanium concentration and the second germanium concentration.

7. The method of claim **6** further comprising:

forming isolation regions in the silicon substrate; and

etching a portion of the silicon substrate between opposite sidewalls of the isolation regions to form a trench, wherein the first silicon germanium layer and the second silicon germanium layer are epitaxially grown in the trench.

8. The method of claim **7** further comprising recessing the isolation regions, so that a top portion of the second silicon germanium layer forms a semiconductor fin, wherein the gate stack comprises a first portion directly over the semiconductor fin, and a second portion on a sidewall of the semiconductor fin.

9. A method comprising:

forming isolation regions in a silicon substrate;

etching a portion of the silicon substrate between opposite sidewalls of the isolation regions to form a first recess;

epitaxially growing a first silicon germanium layer in the first recess, wherein the first silicon germanium layer has a first germanium concentration;

epitaxially growing a second silicon germanium layer in the first recess and over the first silicon germanium layer, wherein the second silicon germanium layer has a second germanium concentration lower than the first germanium concentration;

recessing portions of the isolation regions on opposite sides of the second silicon germanium layer to form a fin, wherein the fin comprises a top portion of the second silicon germanium layer;

forming a gate stack on a top surface and sidewalls of the fin;

forming second recesses on opposite sides of the gate stack, wherein the second recesses penetrate through the second silicon germanium layer and extends into a top portion of the first silicon germanium layer; and

epitaxially growing silicon-containing semiconductor regions in the second recesses to form source/drain regions, wherein the silicon-containing semiconductor regions comprise silicon germanium having a third germanium concentration lower than both the first germanium concentration and the second germanium concentration.

10. The method of claim **9**, wherein the step of epitaxially growing the silicon-containing semiconductor regions comprises growing silicon germanium regions.

11. The method of claim **9**, wherein the step of epitaxially growing the silicon-containing semiconductor regions comprises growing silicon regions that are substantially free from germanium.

12. The method of claim **9**, wherein during the step of epitaxially growing the silicon-containing semiconductor regions, AsH_3 is used as a process gas.

13. The method of claim **1**, wherein the second recess penetrates through the second silicon germanium layer and extends into the first silicon germanium layer.

14. The method of claim **13**, wherein a bottom of the second recess is at an intermediate level between a top surface and a bottom surface of the first silicon germanium layer.

15. The method of claim **6**, wherein the gate stack comprises a gate dielectric, and wherein the gate dielectric is in contact with a top surface of the second silicon germanium layer.